

SH.2
SH.4:2
SH.4:3,4
SH.4
SH.6
SH.4
SH.6:4
SH.4
SH.3
SH.3
SH.4
SH.4:2,6
SH.4:3,6
SH.1:3,4,5,6,8
SH.4:2
SH.4:2
SH.2
SH.2
SH.2

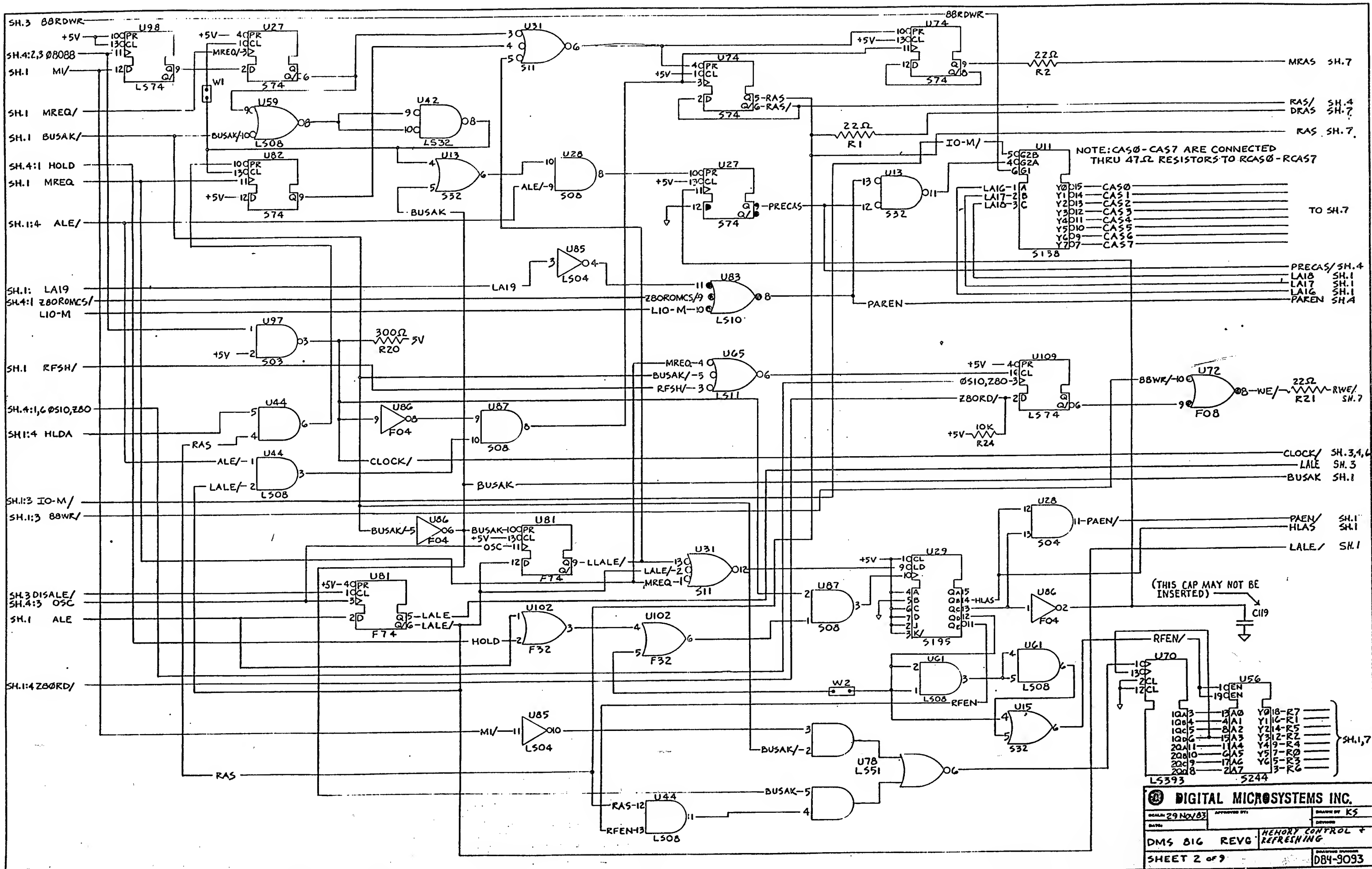
INTA/ L550/ SH.3
LDT-R/ SH.3
D0-D7 SH.3,4,5,8
HLDA SH.2,4
HLDA/ SH.3
IO-M/ SH.2,3
88WR/ SH.2,3,8
MREQ/ SH.2
ALE/ SH.2,4
LA17 SH.2
88RD/ SH.3,4,8
LA18 SH.2
LA16 SH.2
LA19 SH.2
RFSH/ SH.2
AD-A13 SH.8
LA0-7 SH.3,6,8,9
BWDISPSEL/ SH.8
CDISPSEL/ SH.
BWGB45CS/ SH.8
CGB45CS/ SH.
Z80RD/ SH.2,4
DISPSEL/ SH.3,8
IORQ/ SH.4
BUSAK/ SH.2
MREQ/ SH.2
R0-R7 SH.2,7
BWGB45CS/ SH.8
PARRST/ SH.4
CNTRL/ SH.3
CPORT0/ SH.5
CPORT1/ SH.3,5
KI-STAT/ SH.3
NETSET/ SH.6
NMIRST/ SH.4
PEREST/ SH.4
PPORT1/ SH.5
PPORT0/ SH.5
SIOCS/ SH.3,6
SIORST/ SH.4
ZBOSNO/ SH.4
MI/ SH.2
GB45WAIT/ SH.3

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SCALE: DATE: 21 NOV '83 APPROVED BY: DRAWN BY: KS

DMS 816 REV G PROCESSORS, ROM, ADDRESS LATCHING, I/O DECODING

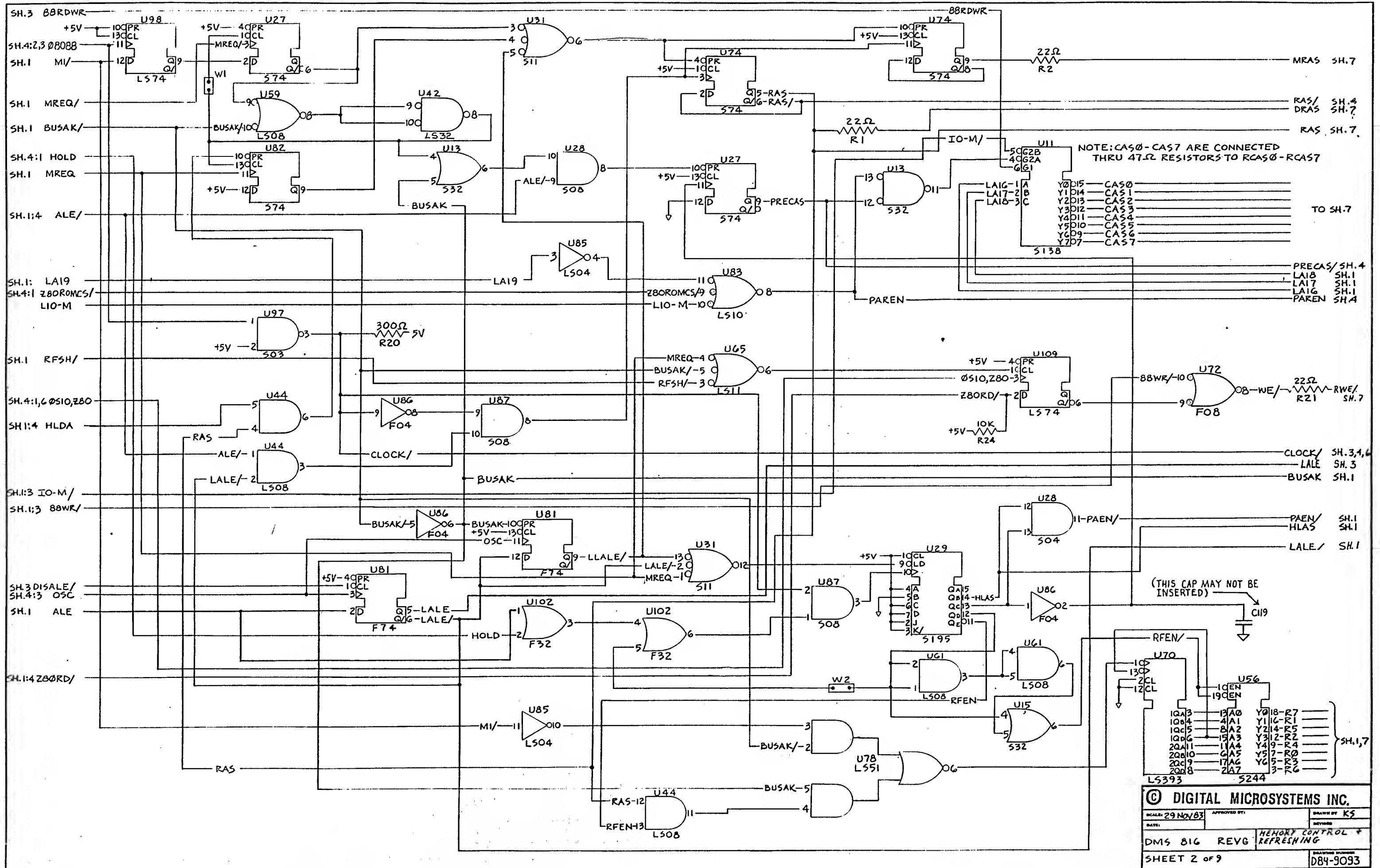
PAGE 1 OF 9 DB4-9093



NOTE: CAS0 - CAS7 ARE CONNECTED THRU 47Ω RESISTORS TO RCAS0 - RCAS7

- Y0D15 - CAS0
- Y1D14 - CAS1
- Y2D13 - CAS2
- Y3D12 - CAS3
- Y4D11 - CAS4
- Y5D10 - CAS5
- Y6D9 - CAS6
- Y7D7 - CAS7

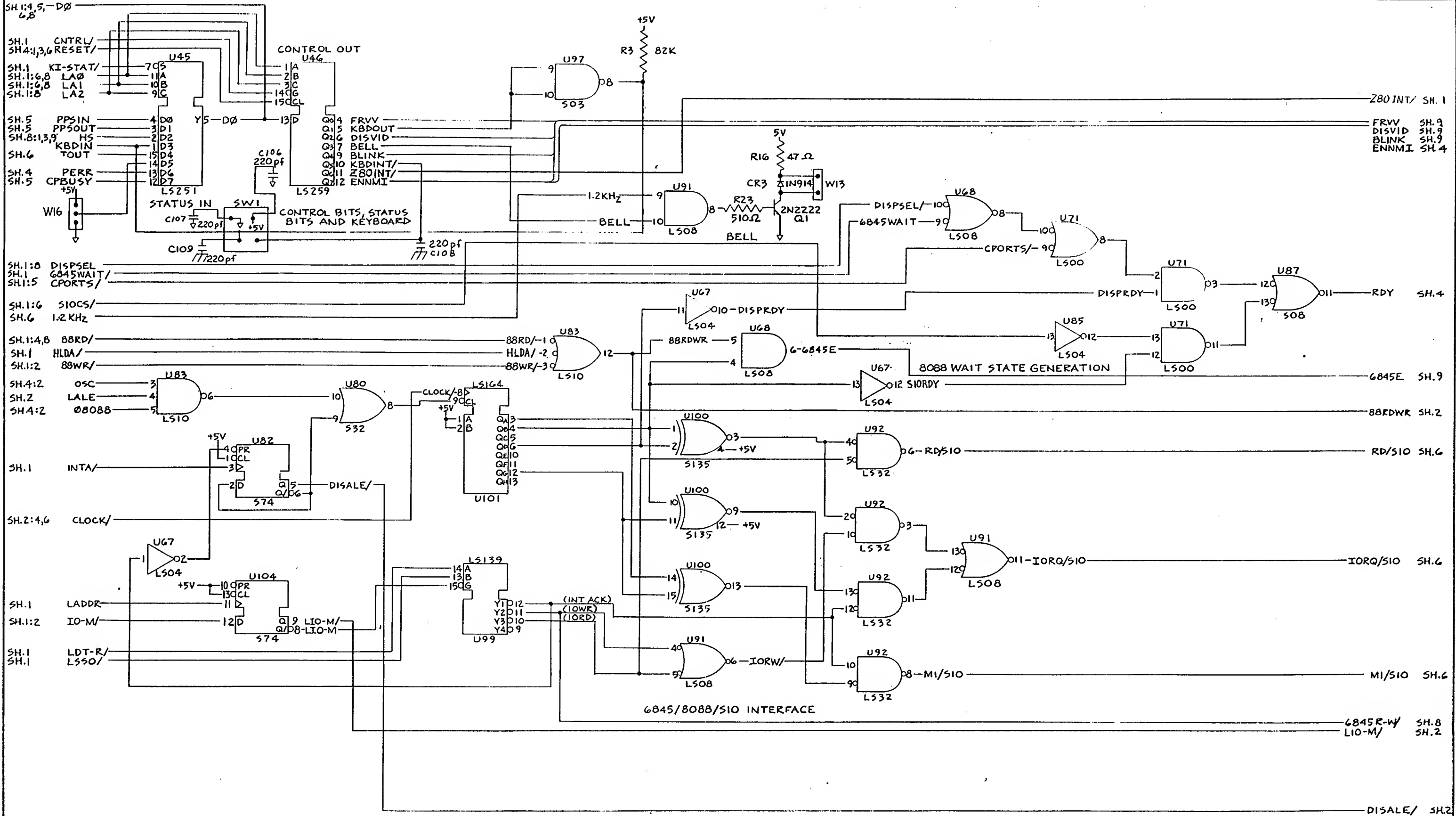
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NOTE: CAS0 - CAS7 ARE CONNECTED THRU 47Ω RESISTORS TO RCAS0 - RCAS7

Y0-D15	CAS0
Y1-D14	CAS1
Y2-D13	CAS2
Y3-D12	CAS3
Y4-D11	CAS4
Y5-D10	CAS5
Y6-D9	CAS6
Y7-D7	CAS7

(THIS CAP MAY NOT BE INSERTED)



SH.1:4,5,-D0
6,8

SH.1 CNTRL/
SH.4:1,3,6 RESET/

SH.1 KI-STAT/
SH.1:6,8 LA0
SH.1:6,8 LA1
SH.1:8 LA2

SH.5 PPSIN
SH.5 PPSOUT
SH.8:1,3,9 HS
SH.6 KBDIN
SH.6 TOUT

SH.4 PERR
SH.5 CPBUSY

SH.1:0 DISPSEL
SH.1 6845WAIT/
SH.1:5 CPORTS/

SH.1:6 SIOCS/
SH.6 1.2 KHz

SH.1:4,8 88RD/
SH.1 HLDA/
SH.1:2 88WR/

SH.4:2 OSC
SH.2 LALE
SH.4:2 08088

SH.1 INTA/

SH.2:4,6 CLOCK/

SH.1 LADDR
SH.1:2 IO-M/

SH.1 LDT-R/
SH.1 L550/

SH.8 6845R-W/ SH.8
SH.2 LIO-M/ SH.2

DISALE/ SH.2

Z80INT/ SH.1

FRVV SH.9
DISVID SH.9
BLINK SH.9
ENNMI SH.4

RDY SH.4

6845E SH.9

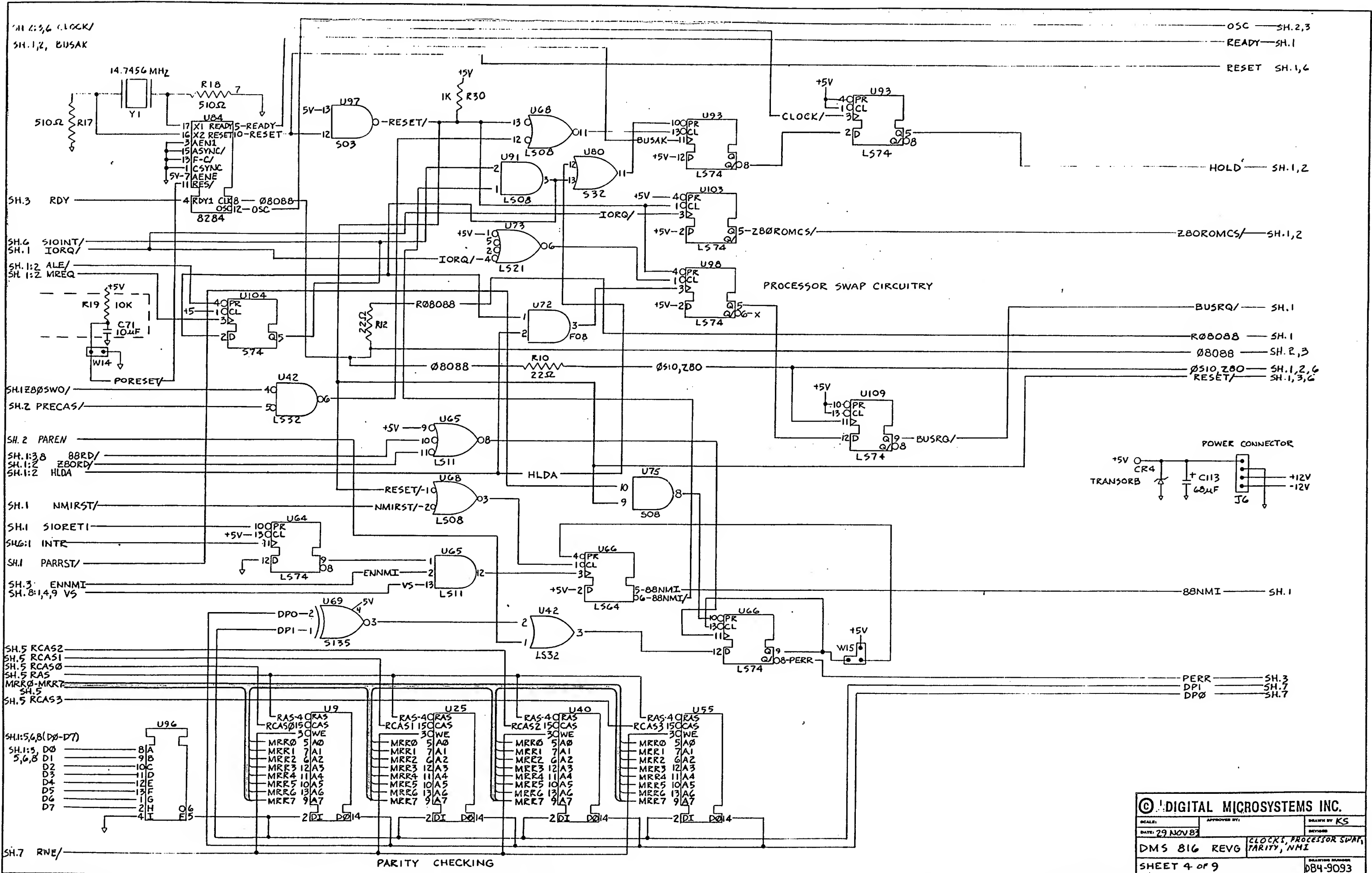
88RDWR SH.2

RD/SIO SH.6

IORQ/SIO SH.6

MI/SIO SH.6

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SCALE:	APPROVED BY:	DRAWN BY KS
DATE: 30 NOV 83		REVISION:
DMS 816 REV G		8088 TO SIO-6845 INTERFACE WAIT STATE (8088) CONTROL + STATUS BITS, KEYBOARD, BELL
SHEET 3 OF 9		DRAWING NUMBER DB4-9093

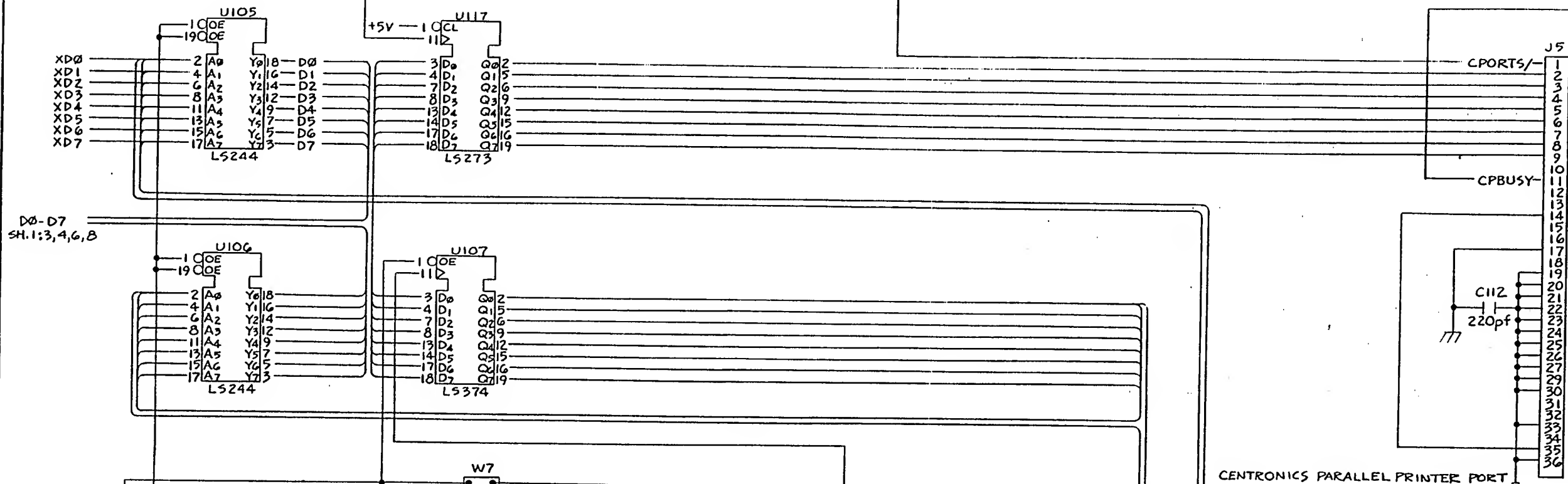


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DATE: 29 NOV 83	REVISION:	
DMS 816 REV G		CLOCKS, PROCESSOR SWAP, PARITY, NMI
SHEET 4 of 9		DATE: 08/93

SH. 1:3
SH. 1

CPBUSY SH. 3.



D0-D7
SH. 1:3,4,6,8

SH. 1 PPORT1/

SH. 1

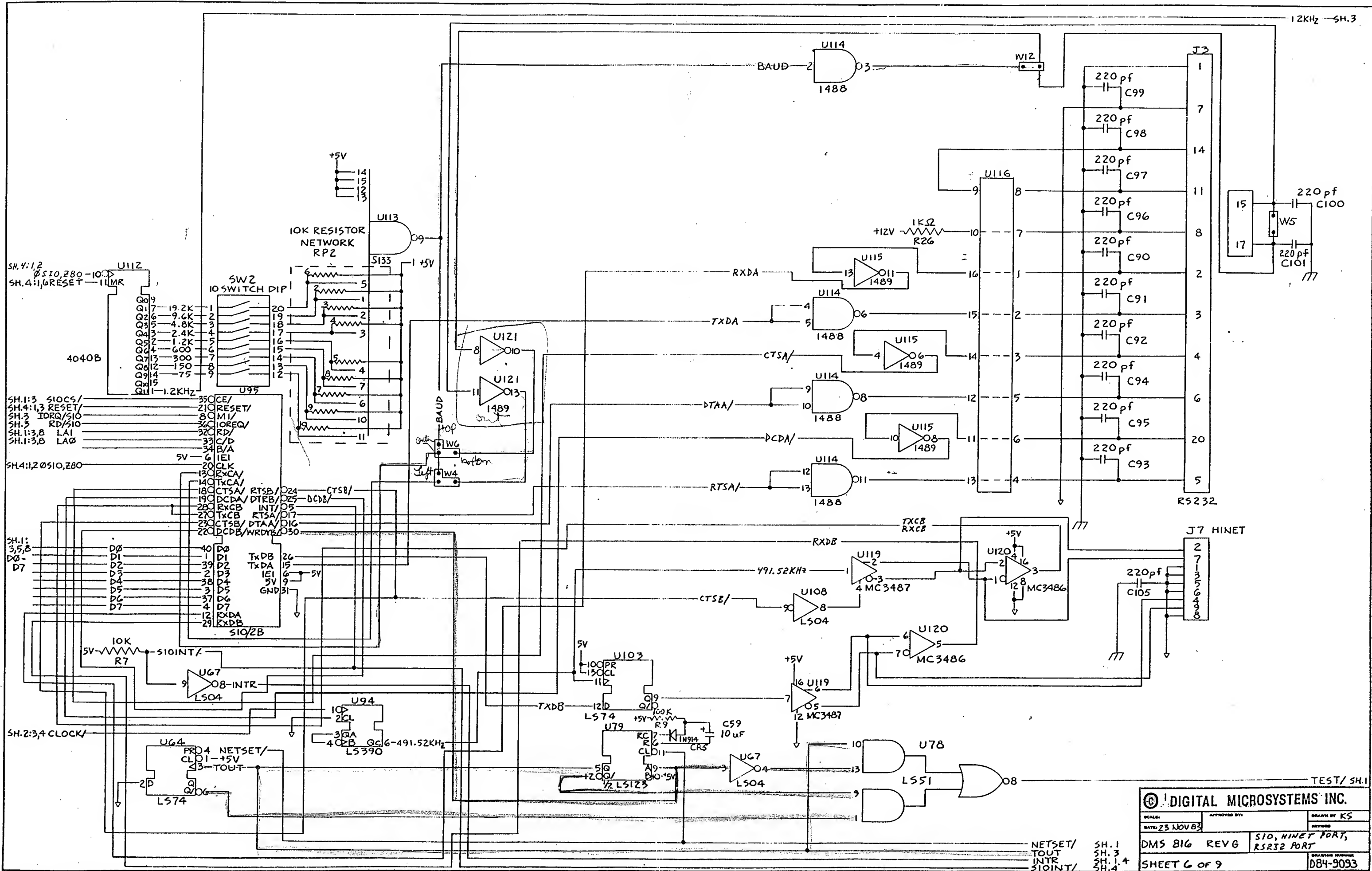
SH. 4:1,3,6 RESET/

CENTRONICS PARALLEL PRINTER PORT

PARALLEL PORT CONNECTOR

PPSOUT SH. 3
PPSIN SH. 3

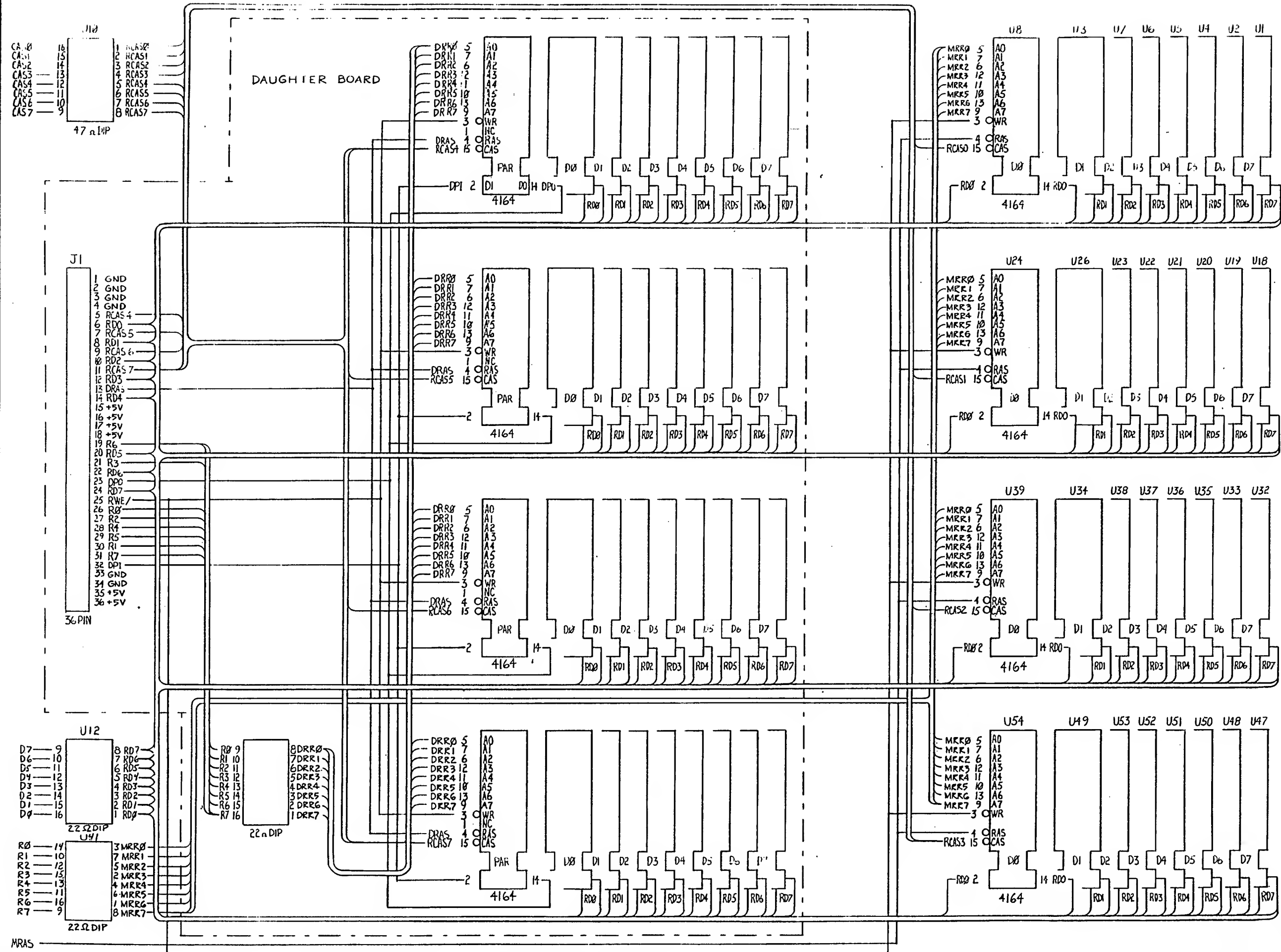
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SCALE: 23 NOV 83	APPROVED BY:	DRAWN BY: KS
DATE: 6 DEC 83	REVISED BY:	REVISED BY:
DMS 816 REV G	PARALLEL PORT CENTRONICS PORT	
SHEET 5 OF 9	DRAWING NUMBER DB4-9093	



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SCALE:	APPROVED BY:	DRAWN BY KS
DATE: 23 NOV 83		REVISION:
DMS 816 REV G	SIO, HINET PORT,	
	RS232 PORT	
SHEET 6 OF 9	DRAWING NUMBER	D84-9093

NETSET/
TOUT
INTR
SIOINT/
SH.1
SH.3
SH.1.4
SH.4

TEST/ SH.1



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SCALE: NONE APPROVED BY: DRAWN BY: B.D.

DATE: 12-22-83

SH 7 OF 9 DMS 816

DAUGHTER & MAIN BD. MEM. DB4-9033